REMARKS

Reconsideration of this application, as amended, is respectfully requested.

In the Office Action, claims 1 and 3-36 were pending. Claims 1 and 3-36 have been rejected.

Claims 1, 3, 15, 23, 34, 35, and 36 have been amended. No claims have been canceled. Claims 37 and 38 have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 103

Claims 1, 3, 8-11, 13-15, and 18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,704,879 to Parrish ("Parrish"), in view of U.S. Patent No. 6,785,829 to George, et al. ("George"), and U.S. Patent No. 6,476,800 to Millman ("Millman").

Amended claim 1 reads as follows:

> A method of managing power in a graphics controller, which is to be coupled to a processor through a bus, comprising:
>
> receiving a change indication related to a system power supply;
>
> adjusting a first clock, wherein the first clock includes a video clock for a display;
>
> adjusting through a voltage regulator, a graphics controller power supply voltage level in response to the receiving of the change indication related to the system power supply; and
>
> informing, by the graphics controller, a Video Graphics Array Basic Input /Output System ("VGA BIOS ") with the change indication related to the system power supply, wherein the informing includes requesting, by the graphics controller, a set of one or more preprogrammed available clock rates stored in the VGA BIOS;
>
> receiving the set of one or more available clock rates;
>
> checking a state of the graphics controller that includes determining whether a 3D engine or 2D engine is active; and
>
> choosing a desired clock rate from the set of available clock rates based on the checking.

(Amended claim 1) (emphasis added)

Parrish discloses a computer system that includes a power source to provide either alternating current ("AC") from an electrical outlet or direct current from a battery (Abstract). More specifically, Parrish discloses that the computer system includes a processor 102 and a graphics adapter 110 coupled through a bus 108 (**Figure 1**). In particular, Parrish discloses that after determining whether the computer system receives power from the AC source, or the battery, processor 102 executes instructions of the graphics BIOS 114 to configure graphics adapter 110 and set the speed of the oscillator to a frequency based on whether the AC source or the battery provides the power to the computer system (col. 2, lines 21-26, **Figure 1**). Importantly, the Examiner's reference to Parrish discloses modifying the frequency of the oscillator when the switch in the power source from AC source to the battery pack or vice versa, is determined (col. 2, lines 45-col. 3, line 7). Further, the Examiner's reference to Parrish discloses setting a frequency of the clock in response to a power level of the battery (col. 4, lines 31-36).

Thus, Parrish merely discloses setting a frequency based on determining whether the AC source or the battery provides the power to the system. In contrast, amended claim 1 refers to requesting, by the graphics controller, a set of one or more preprogrammed available clock rates stored in the VGA BIOS, receiving the set of one or more available clock rates; checking a state of the graphics controller that includes determining whether a 3D engine or 2D engine is active; and choosing a desired clock rate from the set of available clock rates based on such checking.

George, in contrast, discloses adjusting an operating frequency and a supply voltage in sections of a processor based on determining whether the processor is connected to an external power source (Abstract). More specifically, George discloses that the processor includes a graphics controller (**Figures 2 and 3**). The Examiner's reference to George discloses reducing the supply voltage to the graphics controller when the computer is connected to a battery, and

increasing the supply voltage to the graphics controller when the computer is connected to an external power supply (col. 5, lines 28-48). In contrast, amended claim 1 refers to requesting, by the graphics controller, a set of one or more preprogrammed available clock rates stored in the VGA BIOS, receiving the set of one or more available clock rates; checking a state of the graphics controller that includes determining whether a 3D engine or 2D engine is active; and choosing a desired clock rate from the set of available clock rates based on such checking.

Millman discloses the image display system that includes processor 102, display subsystem 110, and display device 112 (**Figure 1**) coupled through a bus 106. More specifically, Millman discloses that the image display system detects the switching between AC-powered and DC-powered operation. In particular, Millman discloses the image display system executes a series of instructions that adjusts the frequency of the video signal of the display subsystem when the system detects switching between the AC powered operation and DC-powered operation (col. 5, lines 48-61).

Thus, Millman merely discloses the image display system that adjusts the frequency of the video signal based on detecting the switch between the AC-powered operation and the DC-powered operation, in contrast to requesting, by the graphics controller, a set of one or more preprogrammed available clock rates stored in the VGA BIOS, receiving the set of one or more available clock rates; checking a state of the graphics controller that includes determining whether a 3D engine or 2D engine is active; and choosing a desired clock rate from the set of available clock rates based on such checking, as recited in amended claim 1.

Thus, neither Parrish, Millman, George, nor any combination thereof, discloses, teaches, or suggest the discussed limitation of amended claim 1.

Therefore, applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103(a) over Parrish, in view of Millman, and further in view of George.

Given that claims 3, 8-11, 13-14 depend from amended claim 1, and add additional limitations, applicants respectfully submit that claims 3, 8-11, 13-14 are not obvious under 35 U.S.C. § 103(a) over Parrish, in view of Millman, and further in view of George.

Amended claim 15 reads as follows:

> A method of effecting power management of a graphics controller, which is to be coupled to a processor through a bus, in an operating system comprising:
>
> programming a set of available clock frequencies and storing the set of the available clock frequencies in a Video Graphics Array Basic Input /Output System ("VGA BIOS ");
>
> detecting a change in a system power supply;
>
> notifying the graphics controller of the change;
>
> receiving an indication of power reduction in the graphics controller, wherein the receiving the indication includes receiving a request from the graphics controller for the set of preprogrammed available clock frequencies stored in the VGA BIOS;
>
> providing the set of available clock frequencies to the graphics controller to choose a desired clock rate from the set of available clock rates based on determining of a state of the graphics controller, wherein the determining of the state includes determining whether a 3D engine or a 2D engine is active, and
>
> adjusting through a voltage regulator a power supply voltage level supplied to the graphics controller in response to the receiving of the indication the power reduction in the graphics controller.

(Amended claim 15)(emphasis added)

Parrish, in contrast, discloses that processor 102 invokes a BIOS routine of a graphics adapter 110 when the power supply changes from AC source to the battery, and fails to disclose receiving a request from the graphics controller for the set of preprogrammed available clock frequencies stored in the VGA BIOS; providing the set of available clock frequencies to the graphics controller to choose a desired clock rate from the set of available clock rates based on determining of a state of the graphics controller, wherein the determining of the state includes determining whether a 3D engine or a 2D engine is active, as recited in amended claim 15.

George, in contrast, discloses reducing the supply voltage to the graphics controller when the computer is connected to a battery, and increasing the supply voltage to the graphics

controller when the computer is connected to an external power supply (col. 5, lines 28-48), and similarly to Parrish, fails to disclose such limitations of amended claim 15.

Millman, in contrast, discloses the image display system that adjusts the frequency of the video signal based on detecting the switch between the AC-powered operation and the DC-powered operation, and similarly to Parrish and George, fails to disclose such limitations of amended claim 15.

As set forth above, neither Parrish, Millman, George, nor any combination thereof discloses such limitations of amended claim15.

Therefore, applicants respectfully submit that amended claim 15 is not obvious under 35 U.S.C. § 103(a) over Parrish, in view of Millman, and further in view of George.

Given that claim 18 depends from amended claim 15, and adds additional limitations, applicants respectfully submit that claim 18 is not obvious under 35 U.S.C. § 103(a) over Parrish, in view of Millman, and further in view of George.

Claims 4, 5, and 12 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Parrish in view of George and Millman, and U.S. Patent No. 5,349,525 to Dunki-Jacobs et al. ("Jacobs").

Dunki-Jacobs, in contrast, discloses an ultrasonic imaging system utilizing a frequency domain wall filter, and similarly to Parrish, Millman, and George, fails to disclose requesting, by the graphics controller, a set of one or more preprogrammed available clock rates stored in the VGA BIOS, receiving the set of one or more available clock rates; checking a state of the graphics controller that includes determining whether a 3D engine or 2D engine is active; and choosing a desired clock rate from the set of available clock rates based on such checking, as recited in amended claim 1.

Given that claims 4, 5, and 12 contain related limitations, applicants respectfully submit that claims 4, 5, and 12 are not obvious under 35 U.S.C. § 103(a) over Parrish, in view of Millman, in view of George, and further in view of Dunki-Jacobs.

Claims 6, 7, 16, and 17 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Parrish, George, Millman, and U.S. Patent No. 6,618,042 to Powell ("Powell").

Powell, in contrast, discloses display brightness control by a processor, and similarly to Parrish, George, Millman fails to disclose the discussed limitations of amended claim 1.

Additionally, Powell, similarly to Parrish, George, and Millman, fails to disclose the discussed limitations of amended claim 15.

Given that claims 6, 7, 16, and 17 depend from amended claims 1 and 15 respectively, and add additional limitations, applicants respectfully submit that claims 6, 7, 16, and 17 are not obvious under 35 U.S.C. § 103(a) over Parrish, in view of Millman, in view of George, and further in view of Powell.

Claims 20-22 and 36 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Parrish, George, Millman, and U.S. Patent No. 5,524,249 to Suboh ("Suboh").

Suboh, in contrast, discloses managing the video subsystem's power by a processor, and similarly to Parrish, George, and Millman fails to disclose the discussed limitations of amended claim 1.

Because claims 20-22 and 36 contain related limitations, applicants respectfully submit that claims 20-22, and 36 are not obvious under 35 U.S.C. § 103(a) over Parrish, in view of George, Millman, and further in view of Suboh.

Claims 23-35 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Parrish, George, Millman, Powell, Dunki-Jacobs, and Suboh.

Amended claim 23 reads as follows:

A graphics controller, which is to be coupled to a processor through a bus, comprising:

a power supply input configured to receive power at a range of voltages from a voltage regulator;

a power supply control output to provide a trigger signal to the voltage regulator to change a voltage level supplied to the graphics controller through the power supply input when a change indication related to a system power supply is detected;

a first clock output that provides an adjustable video clock for a display, and

a system power supply change input coupled to the first clock output and to the power supply control output to detect the change indication related to the system power supply; and

a system interface coupled to the system power supply change input;

a 2D engine;

a 3D engine;

a control unit coupled to the system interface, the 2D engine, and the 3D engine wherein the control unit is configured to inform a Video Graphics Array Basic Input /Output System ("VGA BIOS ") through the system interface about the change indication related to the system power supply, wherein the informing includes requesting a set of one or more preprogrammed available clock rates stored in the VGA BIOS, wherein the control unit is to choose a desired clock rate from the set of available clock rates based on determining of a state of the graphics controller, wherein the determining of the state includes determining whether a 3D engine or a 2D engine is active.

(Amended claim 23) (emphasis added)

As set forth above, Parrish discloses a processor and a graphics adapter that has a graphics BIOS. Further, Parrish rather discloses that a BIOS routine of the graphics adapter is invoked by the processor when the power supply changes from the AC source to the battery. In contrast, amended claim 23 refers to a graphics controller that is to be coupled to a processor through a bus, wherein the graphics controller has a control unit coupled to the system interface, wherein the control unit is configured to inform a Video Graphics Array Basic Input /Output System ("VGA BIOS ") through the system interface about the change indication related to the system power supply, wherein the informing includes requesting a set of one or more

preprogrammed available clock rates stored in the VGA BIOS, wherein the control unit is to choose a desired clock rate from the set of available clock rates based on determining of a state of the graphics controller, wherein the determining of the state includes determining whether a 3D engine or a 2D engine is active.

As set forth above, neither Parrish, George, Millman, Powell, Dunki-Jacobs, Suboh, nor any combination thereof, discloses, teaches, or suggests the discussed limitations of amended claim 23.

Therefore, applicants respectfully submit that claim 23 is not obvious under 35 U.S.C. §103(a) over Parrish, in view of Parrish, George, Millman, Powell, Dunki-Jacobs, and further in view of Suboh.

Because claims 24-36 have related limitations, applicants respectfully submit that claims 24-36 are not obvious under 35 U.S.C. § 103(a) over Parrish, in view of Parrish, George, Millman, Powell, Dunki-Jacobs, and further in view of Suboh.

CONCLUSION

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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